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Ordered Silicon Microwire Arrays Grown from Substrates Patterned Using Imprint Lithography and Electrodeposition

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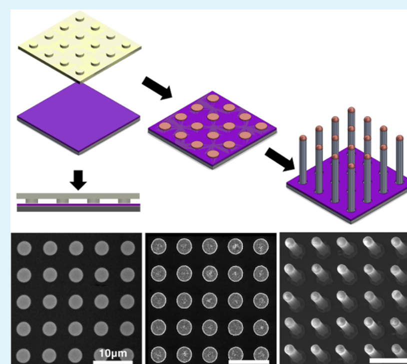
Supporting Information

ABSTRACT: Silicon microwires grown by the vapor−liquid−solid process have attracted a great deal of interest as potential light absorbers for solar energy conversion. However, the research-scale techniques that have been demonstrated to produce ordered arrays of micro and nanowires may not be optimal for use as high-throughput processes needed for large-scale manufacturing. Herein we demonstrate the use of microimprint lithography to fabricate patterned templates for the confinement of an electrodeposited Cu catalyst for the vapor−liquid−solid (VLS) growth of Si microwires. A reusable polydimethylsiloxane stamp was used to pattern holes in silica sol−gels on silicon substrates, and the Cu catalyst was electrodeposited into the holes. Ordered arrays of crystalline p-type Si microwires were grown across the sol−gel-patterned substrates with materials quality and performance comparable to microwires fabricated with high-purity metal catalysts and cleanroom processing.



KEYWORDS: *imprint lithography, electrodeposition, VLS, silicon microwire, photoelectrochemistry*

Silicon microwire (Si MW) and nanowire arrays have a wide range of potential applications for solar energy conversion[1,2] and as components for the next generation of microelectronic and optoelectronic devices.[3] Although the growth and material quality of these arrays has been well-characterized in recent years, few reports have discussed how this technology can be scaled up for large-area manufacturing.[4] The vapor−liquid−solid (VLS) method used to produce Si MW arrays is a robust and scalable approach to the growth of crystalline materials from gaseous precursors.[5] Specifically, the ability to directly produce high-quality, single-crystalline semiconducting material from a low-cost precursor at atmospheric pressure, without the need for further purification or wafering, makes $SiCl_4$ VLS growth an interesting approach for the production of Si for energy-conversion applications.[6−8]

The Si(111) substrate used to produce single-crystal epitaxial growth in the VLS process can be reused if the wires are peeled off in a flexible polymer film and a catalyst metal is subsequently electrodeposited into the remaining oxide pattern.[9,10] However, in all prior reports, the formation of the patterned template relies on high-temperature and high-vacuum processes. For example, oxide-coated (111)-oriented Si growth wafers have been photolithographically patterned to introduce a confining layer that prevents the catalyst droplets from aggregating during VLS growth, and controls the spacing and diameter of the resulting Si microwires (Figure 1).[11] The VLS catalyst material (usually Cu, 99.999%) was then deposited across the entire wafer via thermal evaporation under high vacuum, and the excess metal removed by lift-off in acetone.[11,12] The demonstration that scalable and low-cost patterning and catalyst-deposition techniques can be used to produce controlled microstructures is an important step in the development of scalable Si MW and nanowire technologies. Herein, we report the VLS growth of uniform, position-controlled Si microwires from electrodeposited Cu catalysts on substrates patterned using imprint lithography. Furthermore, we show using photoelectrochemistry that Si MW arrays grown by this method have material quality similar to arrays grown on

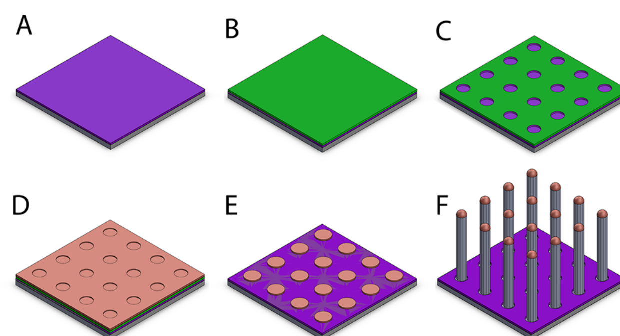


Figure 1. Fabrication process for the growth of Si MW arrays using traditional photolithography and metal catalyst deposition by evaporation. A thermal oxide is (A) grown on a Si wafer (B), coated with photoresist, and (C) patterned using photolithography. (D) A conformal layer of Cu is evaporated over the sample, and then (E) lifted off to leave a patterned substrate for VLS growth. (F) Wires are then grown from $SiCl_4$ using the VLS process.

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substrates prepared with photolithography and high-vacuum metal evaporation. In the present work, we use microimprint lithography, along with subsequent electrodeposition of the metal catalyst, as the process steps used to form a patterned template for VLS-catalyzed Si microwire growth on Si substrates (Figure 2).

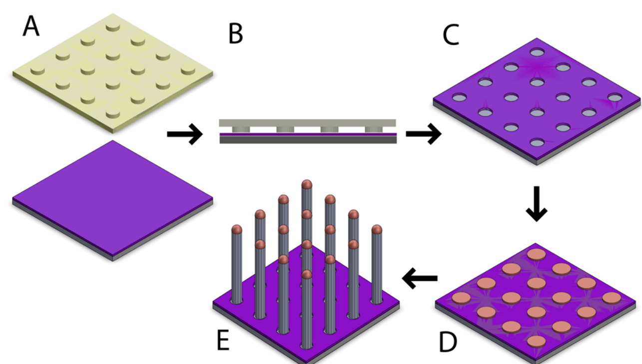

Figure 2. Fabrication process for the growth of Si MW arrays using microimprint lithography and electrodeposition of the metal catalyst. (A) Sol−gel layer is spun onto a Si wafer at a thickness corresponding to that of the imprint stamp, and (B) the stamp is pressed into the sol−gel. (C) Stamp is removed, leaving a pattern of holes in the sol−gel, into which (D) Cu is electrodeposited. (E) Wires are then grown from $SiCl_4$ using the VLS process.

Soft lithography has been used to pattern features less than 100 nm in size, and provides a scalable alternative to traditional photolithography.[13−15] In our work, microimprint lithography of a silica sol−gel was used to create the patterned confining layer on the VLS growth templates. To create the stamp used in the microimprint process, a master was fabricated by photolithographically patterning a thermal SiO_2 layer on a Si wafer. The thickness of the oxide layer was chosen to be the same as the desired thickness of the sol−gel confining layer (∼150 nm), with the pattern specifically consisting of a square-packed array of 3 μm diameter holes spaced 7 μm from center to center (3 × 7 μm^2 pitch). The stamp master was then used to produce a bilayer polydimethylsiloxane (PDMS) stamp that combined a rigid stamping interface with a flexible substrate that allowed for conformal patterning. Each silicon master can be used to produce a large number of flexible PDMS stamps, and each PDMS stamp can be used many times to pattern sol−gel-coated wafers. The rigid stamping PDMS (hereafter referred to as x-PDMS) allowed the stamp to reproduce, with high fidelity, features on the scale of tens of nanometers, whereas the malleable stamp body provided the flexibility necessary to make conformal contact with the substrate.[16]

Before patterning, each Si(111) VLS growth wafer was etched in buffered hydrofluoric acid (BHF), to remove any native oxide. A uniform ∼150 nm thick layer of sol−gel was then produced by spin-coating a silica sol−gel onto the wafer. While the sol−gel was still wet, the bilayer PDMS stamp was carefully applied by hand to cover the entire wafer (Figure 2B). Substrate conformal imprint lithography (SCIL), in which the stamp is attached by a vacuum to a plate that contains a series of grooves that pressurize sequentially to ensure conformal contact between stamp and wafer, and thereby eliminate the defects and air bubbles that are introduced when stamping by hand, could also be used.[17,18] The sol−gel material was allowed to cross-link at room temperature for ∼1 h, and the stamp was carefully removed, resulting in a patterned sol−gel layer. Figure 3 depicts atomic-force microscopy (AFM), scanning-electron

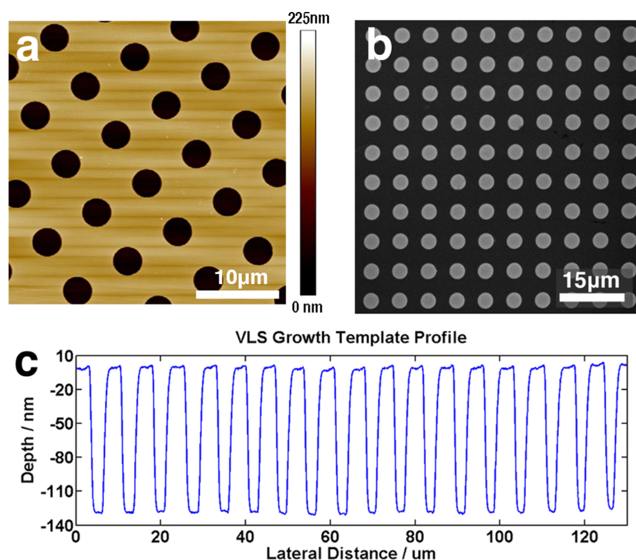

Figure 3. Patterned silica sol−gel on a Si wafer (square packed 3 × 7 μm array of holes): (a) AFM image, (b) SEM micrograph, (c) height measurements from a profilometry line scan.

microscopy (SEM), and contact profilometry images of the templated growth wafers produced by the microimprint lithography process. Using this technique, wafers up to 4" in diameter could be patterned by hand. Because of the flexible nature of the stamp, when macroscopic defects such as air bubbles or dust particles were present, the pattern quality was only affected locally (over a range of μm to mm from the defect), so the stamp was replicated in the sol−gel over >90% of the substrate even when the substrates were not patterned in a cleanroom.

During the VLS growth process, the patterned substrate is exposed to 1000 °C and to flowing $H_2(g)$ and $SiCl_4(g)$. These conditions create HCl(g) as a byproduct, and therefore require a robust patterned confining layer. To determine whether the sol−gel would retain its pattern fidelity during the wire-growth process, pieces of a patterned Si wafer were annealed under $N_2(g)$ for 20 min at temperatures between 100 and 1000 °C. Profilometry of the annealed samples showed a slight densification of the sol−gel, but indicated the general retention of the stamped pattern. A substrate chip with a patterned sol−gel (but without the VLS growth catalyst) was also placed into the chemical-vapor deposition (CVD) reactor and sent through the growth process with all variables intact, except for the absence of $SiCl_4(g)$ and $BCl_3(g)$ during the "growth" phase of the process. Despite the gas flows and high temperatures, a slight compaction (<10%) of the sol−gel was observed but the pattern fidelity remained high, confirming that the sol−gel could be used to replace the confining thermally grown SiO_2 layer that has been previously used to produce Si microwire arrays.[11]

The VLS growth process also requires use of a metal catalyst, typically either Cu, Ni, or Au. The purity of the metal used as the VLS catalyst affects the device performance of the resulting Si MW arrays.[19,20] Cu impurities are less detrimental than Au impurities to the performance of both planar and microwire Si solar cells, motivating the investigation of electrodeposited Cu

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as an alternative VLS catalyst.[21,22] We therefore focused our effort on enabling the use of Cu for the growth of VLS-catalyzed Si MW arrays.

To achieve conformal electrodeposition of Cu and thus high-quality VLS Si MW growth, the sol−gel was first densified by baking the substrate on a hot plate at 150 °C for 20 min, and then the residual sol−gel and native oxide were removed from the patterned holes by dipping the substrate in dilute HF (aq, 1% by volume). Although the sol−gel slowly etches in HF(aq), careful control over the duration of this etch allowed for exposure of the conductive Si substrate at the bottom of the holes while not impacting the quality of the SiO_2 confining layer elsewhere.

Immediately after etching, the patterned wafer was placed into a pressed electrodeposition cell that had been filled with a commercially available copper electrodeposition solution (see Figure S1 in the Supporting Information). A high-purity Cu (99.9999%) rod served as the counter electrode. Cu was then deposited potentiostatically at −1.05 V vs Ag/AgCl until the desired charge density had been passed. Optical microscopy and SEM images indicated that the Cu deposited selectively in the holes in the patterned overlayer, with excellent fidelity across large (>3 cm^2) areas (Figure 4).

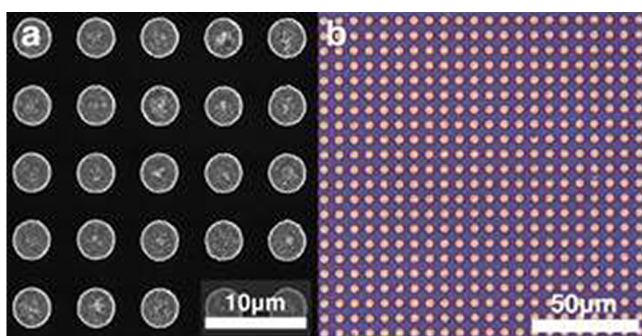

Figure 4. (a) SEM and (b) optical images of electrodeposited copper in patterned sol−gel. Diameter = 3.5 μm, pitch = 7 μm.

Samples were then placed into the CVD reactor, to grow p-type Si MW arrays. Wire growth was performed at 1000 °C in H_2(g), using $SiCl_4$(g) as the Si precursor and BCl_3(g) as the p-type dopant source. The passage of ~0.2 C cm^{-2} of charge density during Cu electrodeposition resulted in wires that were 2 μm in diameter. The diameter of the wires depended on the diameter of the hemispherical catalyst eutectic droplet formed during growth, hence the wire diameter was different than that of the catalyst island.[12] The dopant density of the wires was ~6 × 10^{17} cm^{-3}, as measured using a 4-point probe technique.[23] The wires grown from the electrodeposited catalyst exhibited uniformity across the growth substrate comparable to substrates patterned with photolithography (Figure 5). The amount of electrodeposited copper determined the diameter of the resulting Si MWs, hence given the flexibility afforded by electrodeposition, large amounts of material could be quickly and easily deposited to thereby permit the controlled growth of Si MWs of various diameters (see the Supporting Information).

To evaluate the electrical performance of the microwire arrays, the wires were cleaned using an RCA2 etch to remove the Cu growth catalyst and other impurities, and the substrate-supported wire arrays were then processed and made into electrodes. Additional processing was required for evaluation of

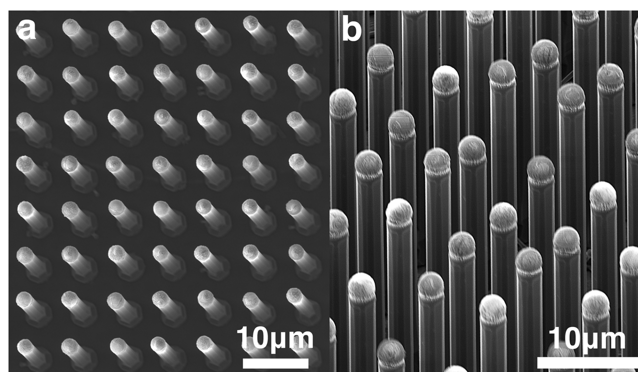

Figure 5. SEM micrographs of Si MW arrays grown from electrodeposited Cu and silica sol−gel patterned substrates. (a) Top down view of as-grown wires (before catalyst removal), (b) 45° tilt view of as-grown Si MW array.

the performance of MWs on the Si substrate, because the degenerately doped growth wafer and the microwire bases can provide pathways for shunting during electrochemical testing of the performance of the Si MW arrays. To protect these interfaces from the electrolyte, an oxide boot was formed on the microwires (see Figure S2 in the Supporting Information), by growth of a ~ 150 nm thick thermal oxide over the entire surface of the sample at 1000 °C for 2 h.[24] The oxide was selectively protected at the wire bases and growth substrate, and was etched off everywhere else. This oxidation process is also thought to act as a getter for metallic impurities incorporated at the surface of the wires as a result of the metal-catalyzed growth process, and etching of this oxide layer is equivalent to removing the outer 50−100 nm of the metal-rich Si surface layer and results in improved photoelectrochemical performance of the wire arrays.[1]

The resulting Si MW arrays were then made into electrodes, and tested for their photoelectrochemical performance in contact with a 50 mM solution of the one-electron, reversible, methyl viologen ($MV^{2+/+}$) redox couple.[25,26] The $MV^{2+/+}$ redox couple makes a conformal, high barrier-height contact to p-type Si, and has been used to study the performance of similar p-Si MW arrays (see the Supporting Information for experimental details and controls).[1,24] At normal incidence under 60 mW cm^{-2} of 808 nm illumination (which produces a similar photon flux above the Si band gap as that obtained from broadband, 100 mW cm^{-2}, AM 1.5G solar illumination), the champion Si MW electrode grown from microimprint/electrodeposition exhibited an open-circuit voltage (V_{oc}) = 400 ± 7 mV, a short-circuit current density (J_{sc}) = 6.8 ± 0.5 mA cm^{-2}, an external quantum yield at short circuit ($\Phi_{ext,sc}$) = 0.17 ± 0.02, a fill factor (ff) = 0.52 ± 0.03 and an energy-conversion efficiency (η_{808}) = 2.4 ± 0.2% (Figure 6). Averaging across six devices, the figures of merit for the Si microwire arrays under investigation were V_{oc} = 380 ± 10 mV, J_{sc} = 7 ± 2 mA cm^{-2}, $\Phi_{ext,sc}$ = 0.17 ± 0.05, ff = 0.5 ± 0.1, and η_{808} = 2.1 ± 0.3%. These figures of merit are comparable to those of Si microwires grown from photolithographically patterned oxide templates and thermally evaporated high-purity Cu, with the largest difference arising from the open-circuit voltage, which was only ~30 mV smaller than that observed for wires grown with 6N Cu.[1] This trend contrasts with that observed for Au-catalyzed Si MW arrays, in which a slight decrease in the purity of the Au used (5N vs 6N) led to a significant reduction in the photoelectrochemical energy-conversion efficiency of the resulting Si MW arrays.[20]

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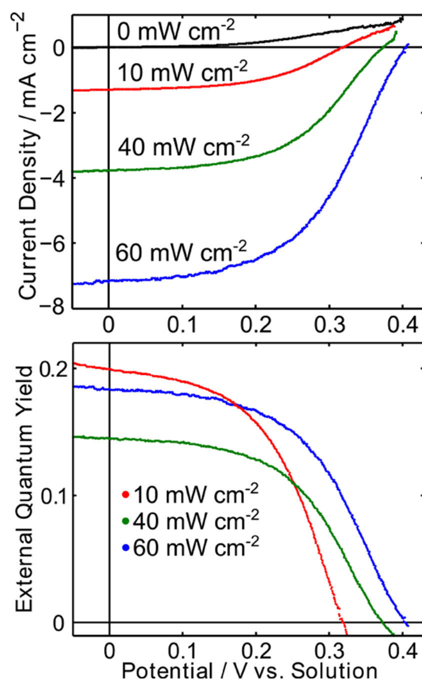

Figure 6. (Top) *J*–*E* data and (bottom) external quantum yield for Si MW array electrodes tested in 50 mM $MV^{2+/+}$ electrolyte under 808 nm illumination.

The external quantum efficiency of the electrode for wavelengths from 400 to 1100 nm was measured as a function of the angle of incidence of light relative to the surface of the Si substrate. As shown in Figure 7, measurements were obtained

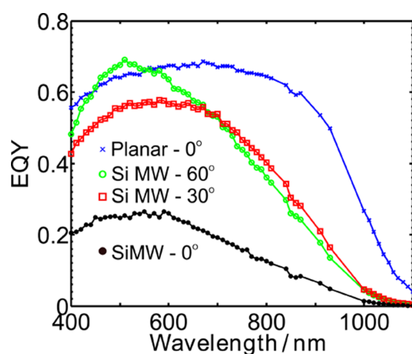

Figure 7. Spectral response of p-Si MW array and planar p-Si electrodes measured in methyl viologen electrolyte. Data were obtained under potentiostatic conditions at the light-limited photocurrent (−0.5 V vs SCE).

at 0 (approximately normal to the array), 30, and 60°, respectively. The spectral response of the wire arrays that were grown from the templating method described herein was nearly identical to that of wire arrays grown from 6N Cu with the pattern introduced into a thermal SiO_2 overlayer using photolithography.[27]

In summary, a scalable, low-cost, and low-energy fabrication technique for the growth of vertically oriented silicon microwire arrays has been demonstrated, resulting in the production of Si microwire arrays with essentially equivalent electrical performance to wire arrays produced using traditional high-energy, higher-cost fabrication methods. Patterning of the growth substrate was accomplished via microimprint lithography using a silica sol–gel, and catalyst deposition was achieved by potentiostatic electrodeposition from commercially available Cu electrodeposition solutions. This fabrication method is both scalable and robust, allowing for the creation of Si microwire arrays of varying pitch and wire diameter, which can potentially lead to the fabrication of more efficient photocathodes for the hydrogen-evolution reaction (HER) and/or form the basis for new sensors and battery electrodes made from Si microwire and nanowire arrays.

■ ASSOCIATED CONTENT

Supporting Information

Detailed experimental methods including the fabrication of the microimprint stamps, the electrodeposition of Cu, and the processing of the wire arrays are provided. This material is available free of charge via the Internet at http://pubs.acs.org.

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The manuscript was written through contributions of all authors. All authors have given approval to the final version of the manuscript.

Notes

The authors declare no competing financial interest.

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■ ABBREVIATIONS

VLS, vapor–liquid–solid
Si MW, silicon microwires
PDMS, polydimethylsiloxane
BHF, buffered hydrofluoric acid
AFM, atomic-force microscopy
SCIL, substrate conformal imprint lithography
SEM, scanning-electron microscopy
CVD, chemical-vapor deposition

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